CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. –59. (Cancelled)

60. (New) An apparatus, comprising

a power input to receive a supply voltage;

core logic to execute functions, the core logic coupled to the power input to receive the supply voltage to power operation of the core logic;

a voltage controlled oscillator ("VCO") circuit coupled to the power input to receive the supply voltage and to generate a clock signal for the core logic having a first frequency dependent upon a level of the supply voltage; and

a frequency control circuit to produce select signals to select the level of the supply voltage.

61. (New) The apparatus of claim 60, wherein the frequency control circuit includes a temperature sensor to sense a temperature about the core logic, the frequency control circuit to select the level of the supply voltage based at least in part upon a present temperature sensed by the temperature sensor.

62. (New) The apparatus of claim 61, wherein the VCO circuit comprises:

a plurality of distributed oscillators each coupled to receive the supply voltage from the power input and to generate the clock signal dependent upon the supply voltage; and

a clock distribution network coupled to the plurality of distributed oscillators to distribute the clock signal to the core logic.

63. (New) The apparatus of claim 62, further comprising a power distribution network coupled to the power input to distribute the supply voltage to the plurality of distributed oscillators and to the core logic.

64. (New) The apparatus of claim 62, wherein the plurality of distributed oscillators comprises a plurality of distributed ring oscillators.

65. (New) The apparatus of claim 62, wherein each of the plurality of distributed oscillators includes a select circuit to select between a synchronous mode to drive the clock distribution network and an asynchronous mode to drive the clock distribution network.

66. (New) The apparatus of claim 65, wherein the select circuit comprises a multiplexer coupled to output a feedback clock signal when the asynchronous mode is selected and coupled to output an external clock signal when the synchronous mode is selected.

67. (New) The apparatus of claim 61, wherein the core logic comprises a processor core.

68. (New) The apparatus of claim 67, further comprising a software selectable switch to select between at least a frequency maximizing mode of operation and a power minimizing mode of operation of the processor core.

69. (New) The apparatus of claim 61, further comprising:

a divide-by-N circuit coupled to receive the clock signal from the VCO circuit and to generate a divide signal having a second frequency substantially equal to the first frequency divided by N; and

a comparator coupled to receive the divide signal and an external clock signal, the comparator to generate a feedback signal based on a comparison of the divide signal and the external clock signal, the frequency control circuit coupled to receive the feedback signal and to select the level of the supply voltage at least in part upon the feedback signal.

70. (New) The apparatus of claim 69, wherein the comparator comprises a frequency comparator.

71. (New) The apparatus of claim 69, wherein the frequency control circuit comprises a voltage ID ("VID") controller to couple to a VID bus, wherein the select signal comprises a VID signal to be asserted onto the VID bus to control a voltage regulator.

72. (New) A method, comprising:

powering an integrated circuit ("IC") with a supply voltage to provide operational power to logic components of the IC;

generating a clock signal having a frequency dependent upon a level of the supply voltage; and

clocking the logic components with the clock signal.

73. (New) The method of claim 72, further comprising:

selecting the level of the supply voltage to select a desired frequency of the clock signal.

74. (New) The method of claim 73, wherein selecting the level of the supply voltage further comprises:

dividing the clock signal by N to generate a divided clock signal;

comparing the divided clock signal with an external clock signal;

generating a feedback signal based upon the comparing; and

selecting the level of the supply voltage at least in part based upon the feedback signal.

75. (New) The method of claim 73, wherein selecting the level of the supply voltage comprises:

sensing a temperature about the logic components; and

selecting the level of the supply voltage based at least in part upon the temperature about the logic components.

76. (New) The method of claim 75, further comprising selecting a maximum level of the supply voltage to select a maximum frequency of the clock signal based at least in part on the sensed temperature about the logic components to operate the logic components in a frequency maximizing mode.

77. (New) The method of claim 73, further comprising selecting a minimum level of the supply voltage to select a minimum frequency of the clock signal to operate the logic components in a power minimizing mode.

78. (New) The method of claim 73, wherein the IC comprises a processor and the logic components comprise a core of the processor.